Performance of Low Power BIST Architecture for UART

Abstract—

Universal Asynchronous Receiver Transmitter (UART) is used for exchanging data between computer and peripherals at a very short distance. In this paper, Built in Self Test (BIST) architecture with Bit Swapping Linear Feedback Shift Register (BS-LFSR) is used for testing UART. Generally, BIST for UART consists of test patterns obtained from conventional LFSR. BS-LFSR consists of shift registers, Multiplexers and a XOR logic gate. Pattern generation in BSLFSR is similar to the normal LFSR but the sequence of the test pattern will be different. This method reduces the power consumption during testing of circuits by reducing number of switching activities when compared to the conventional LFSR. In the Bit-swapping LFSR maintaining randomness in the test pattern generation is the most important factor. Because of this randomness it gives high fault coverage. The main advantages of this work are better power reduction and less hardware requirement.

**LANGUAGE USED:**

**TOOLS REQUIRED:**

* MODELSIM – Simulation
* XILINX-ISE – Synthesis